**LESSON PLAN**

**Subject Code & Name: EDA Tools**

**Branch: VLSI & DECS Class / Semester: IM.Tech-SEM 1 Academic Year:2015-16**

**Faculty: B.Rama rao**

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| **Period** | **Date (Tentative)** | **Topic** | **Unit No.** | **Teaching Methodology** | **Remarks** | **Corrective action upon review** |
|  |  | **Important concepts in verilog** | **I** |  |  |  |
| 1 | 17.11.2015 | Introduction |  | BB |  |  |
| 2 | 18.11.2015 | Basics of verilog language |  | BB |  |  |
| 3 | 19.11.2015 | Operators,heirarchy |  | BB |  |  |
| 4 | 21.11.2015 | Procedures and assignments |  | BB |  |  |
| 5 | 24.11.2015 | Timing controls and delay |  | BB |  |  |
| 6 | 25.11.2015 | Tasks and function control statements |  | BB |  |  |
| 7 | 26.11.2015 | Logic gate modeling Delay, |  |  |  |  |
| 8 | 28.11.2015 | Alternating parameters and other parameters |  |  |  |  |
|  |  | **Synthesis ansd simulation using HDLS-I** | **II** |  |  |  |
| 9 | 01.12.2015 | Verilog and logic synthesis |  | BB |  |  |
| 10 |  | VHDL and logic synthesis |  | BB |  |  |
| 11 | 02.12.2015 | Memory synthesis |  | BB |  |  |
| 12 | 03.12.2015 | FSM synthesis |  | BB |  |  |
| 13 | 05.12.2015 | Performance driven synthesis |  | BB |  |  |
| 14 | 08.12.2015 | Types of simulation |  | BB |  |  |
| 15 | 09.12.2015 | Logic systems, |  |  |  |  |
| 16 | 10.12.2015 | Logic simulation |  |  |  |  |
|  |  | **Synthesis ansd simulation using HDLS-I**I | **III** |  |  |  |
| 17 | 12.12.2015 | Cell models |  | BB |  |  |
| 18 | 16.12.2015 | delaymodels |  | BB |  |  |
| 19 | 17.12.2015 | State timing analysis |  | BB |  |  |
| 20 | 19.12.2015 | Formal verification |  | BB |  |  |
| 21 | 22.12.2015 | Switch Level simulation |  | BB |  |  |
| 22 | 23.12.2015 | transistor Level simulation |  |  |  |  |
| 23 | 24.12.2015 | CAD tools for Synthesis and simulation |  |  |  |  |
| 24 | 26.12.2015 | leonardo spectrum |  |  |  |  |
|  |  | **Tools for circuit design and simulation using PSPICE** | **IV** |  |  |  |
| 25 | 29.12.2015 | Introduction |  |  |  |  |
| 26 | 30.12.2015 | PSPICE models for transistors |  | BB |  |  |
| 27 | 30.12.2015 | A/D ,D/A, sample annd hold circuits |  | BB |  |  |
| 28 | 31.12.2015 | Digital sys building blocks |  | BB |  |  |
| 29 | 02.01.2016 | Design and analysis of digital circuits using PSPICE |  | BB |  |  |
| 30 | 19.01.2016 | Design and analysis of analog circuits using PSPICE |  | BB |  |  |
| 31 | 20.01.2016 | PSPICE examples |  | BB |  |  |
|  |  | **An overview of mixed signal VLSI design** | **V** |  |  |  |
| 32 | 21.01.2016 | Fundamentals of analog and digital simulation |  | BB |  |  |
| 33 | 23.01.2016 | Mixed signal simulator configurations |  | BB |  |  |
| 34 | 26.01.2016 | Understanding modellings |  | BB |  |  |
| 35 | 27.01.2016 | Integration to CAE environments |  | BB |  |  |
| 36 | 28.01.2016 | Analysis of analog circuits |  | BB |  |  |
| 37 | 30.01.2016 | A/D ,D/A converters |  | BB |  |  |
| 38 | 02.02.2016 | Up/down converters |  | BB |  |  |
| 39 | 03.02.2016 | compounders |  | BB |  |  |
|  |  | **Tools for PCB design and layouts** | **VI** |  |  |  |
| 40 | 06.02.2016 | Introduction |  | BB |  |  |
| 41 | 09.02.2016 | An overview of high speed PCB design |  | BB |  |  |
| 42 |  | Design entry |  | BB |  |  |
| 43 | 10.02.2016 | Simulation and layout tools for PCB |  | BB |  |  |
| 44 | 11.02.2016 | and layout tools for PCB |  | BB |  |  |
| 45 | 13.02.2016 | Introduction to ORCAD PCB Design tools |  | BB |  |  |
| 46 | 17.02.2016 | ORCAD PCB |  | BB |  |  |

**CR: CLASS ROOM PPT: POWER POINT PRESENTATION LCD**

**TEXT BOOKS:**

1. Z. Kohavi – “Switching & finite Automata Theory” (TMH).

2. N. N. Biswas – “Logic Design Theory” (PHI).

3. Nolman Balabanian, Bradley Calson – “Digital Logic Design Principles” – Wily Student Edition

2004.

**REFRENCE BOOKS:**

1. M. Abramovici, M. A. Breues, A. D. Friedman – “Digital System Testing and Testable Design”,

Jaico Publications.

2. Charles H. Roth Jr. – “Fundamentals of Logic Design”.

3. Frederick. J. Hill & Peterson – “Computer Aided Logic Design” – Wiley 4th Edition.

**FACULTY HEAD OF THE DEPARTMENT**